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Ultra-Thin Silicon based Piezoelectric Capacitive Tactile Sensor

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Abstract

This paper presents an ultra-thin bendable silicon based tactile sensor, in a piezoelectric capacitor configuration, realized by wet anisotropic etching as post-processing steps. The device is fabricated over bulk silicon, which is thinned down to 35 µm from an original thickness of 636 µm. Dicing of thin membrane is achieved by low cost novel technique of Dicing before Etching. The piezoelectric capacitor is composed of polyvinylidene fluoride trifluoroethylene (PVDF-TrFE), which present an attractive avenue for tactile sensing as they respond to dynamic contact events (which is critical for robotic tasks), easy to fabricate at low cost and are inherently flexible. The sensor exhibits enhanced piezoelectric properties, thanks to the optimization of the poling procedure. The sensor capacitive behaviour is confirmed using impedance analysis and the electro-mechanical characterization is done using TIRA shaker setup.

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Keywords: Flexible Electronics; Tactile Sensor; Micro-Machining; Ultra-Thin Chips

1. Introduction

The market share of flexible electronics is thriving high and expected to reach a billion-dollar mark by 2020 [1]. With application ranging from flexible RFID patches to flexible photovoltaics in high-tech space applications, there is expectation that the use of flexible electronics will increase further. One of the applications that has gained significant interest over the time is the large area electronic or tactile skin (e-Skin), which is multiple sensing (e.g. humidity, tactile, temperature sensing etc.) and electronic components integrated on flexible substrate to provide

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human-skin like feelings in robotics or to monitor health parameters [2, 3]. While sensors for humidity etc. can be discretely distributed, the tactile and temperature sensing needs to be integrated all over the e-skin, with different resolutions at different locations [4]. For this reason the tactile sensors make the most important part of e-skin.

An ideal tactile sensor for its application in e-skin is expected to be thin, flexible, distributed over large area with high resolution, resistant to chemicals and durable to external force [5]. Over the past two and a half decades, the pursuit to meet above needs and improvements in tactile sensing capability has resulted in many kind of touch sensors, exploring numerous modes of transductions including piezoresistive, capacitive, piezoelectric, magnetic and optical modes of transduction [4]. The organic based sensors and electronics have also been explored as they provide the mechanical flexibility and conformability, but their use is limited by the lower performance [6]. On the contrary, MEMS based sensors which uses brittle materials like PZT, AlN, silicon as transducer reports high performance but lacks flexibility [7]. The tactile sensors based on soft piezo-polymer polyvinylidene fluoride (PVDF) and its copolymer polyvinylidene fluoride trifluoroethylene P(VDF-TrFE) have been developed for various applications like medical sciences, robotics, space technology and many more [8, 9]. One of the tactile sensors which combines high piezoelectric coefficient P(VDF-TrFE) with high performance silicon based transistor is based on Piezoelectric Oxide Semiconductor Field Effect Transistor (POSFET). This device brings the sensing and conditioning unit together and has shown good sensitivity to dynamic force [10, 11]. However, being fabricated on standard silicon wafer, it application in flexile electronics is limited [12]. Research is going on in our group towards realization of flexible silicon based devices and sensors [13, 14], and the work presented here is a step towards achieving this goal.

2. Device Fabrication

The capacitors are fabricated on a <100> double side polished 6 inch p-type silicon wafers with resistivity $10 \sim 20\ \Omega.\mathrm{cm}$ and initial thickness 636 µm. The double side polished wafer are chosen to ensure high level of smoothness on the etched surface and thus keep the stress level low.

As shown in Fig. 1(i), the process starts with depositing silicon oxide-silicon nitride-silicon oxide stack by LPCVD method. The stack is composed of 1200 nm layer of SiO_2, 80 nm layer of Si_3N_4 and 800 nm layer of SiO_2. This stack

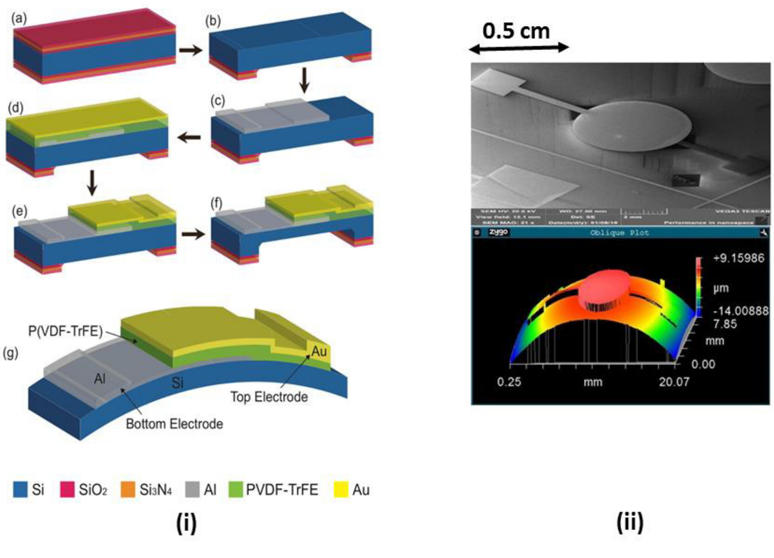

Fig.1: **(i)** Fabrication steps for obtaining ultra-thin silicon based piezo-capacitors: (a) Hard mask growth (b) Patterning backside to open etching window (c) Bottom metal deposition and patterning (d) PVDF-TrFE spin coating, annealing and top metal deposition (e) Patterning top metal and dry etching of polymer (f) Wet etching of bulk silicon (g) Final device on thin silicon **(ii)** (top) SEM image of the piezo-capacitors sensor (bottom) Optical profilometer image of thin chip with piezo-capacitor showing warpage.

acts as hard mask for patterning of the etching window needed during wet etching. Front side stack is dry etched and PECVD SiO_2 is grown to reduce number of stress layers. A 600 nm aluminum film is deposited via sputtering and patterned to make the bottom electrode of capacitor. Commercially available P(VDF-TrFE) pellets were dissolved in RER 500 solvents using magnetic stirrer at 80^0C to obtain 10 wt% solution. The solution was spin coated over the patterned wafer and thickness measured with optical interferometer was found to be 2µm. This was also confirmed with ellipsometer.

Since piezoelectric property of polymer depends on its crystal structure, the crystallinity was improved by annealing the polymer film in nitrogen atmosphere. Gold (Au) metal of thickness 150 nm was deposited and patterned to realize top electrode of the capacitor. Following this, the P(VDF-TrFE) was etched using oxygen plasma. Wherever the top Au electrode was present, it acted as the protecting mask and prevented the polymer from getting etched. The SEM image of the piezoelectric capacitive structure over bulk silicon is shown in Fig. 1(ii).

After front end fabrication, post processing was carried out to realize ultra-thin capacitive structure. Wafer was partially diced, with the dicing depth deciding the final thickness of the thin chips. Wet etching using 25% TMAH solution is chosen because of its ability to give very low sub surface damage (SSD) and thus very smooth etched surface. Etching was carried out at 90^0C, which gives etching rate of 40 µm/hr. When the etching depth reaches the dicing cut depth, die separation occurs automatically. Holder with separated chips is taken out immediately out of the TMAH bath, and rinsed and left for drying. Dies are separated using vacuum pick-up system. Slight warpage is observed in the chip as shown in Fig. 1 (ii). This is because of stress generated in the chip after thinning.

Poling of P(VDF-TrFE) film is performed by step-wise poling method at elevated temperature [11]. This ensures the dipole alignment in field direction and thus improves the piezoelectric property of the polymer.

3. Device Characterization

3.1. Electrical Impedance Spectroscopy

Electrical impedance spectroscopy (EIS) involves the measurement of the output electrical potential (V_{out}), and the phase shift (φ) of a system when an alternating current of small amplitude (I_{out}) and known frequency ω is applied. An impedance analyzer (HP LF 41928) is used to measure the impedance of the piezo capacitor over a frequency range of 5 Hz–10MHz. As shown in Fig. 2(i), capacitive behavior is observed over a large frequency range. The capacitance value can be calculated by fixing a frequency. The value of capacitance is also confirmed by Casace MircoTech PM5 probe station. The measured value is 1.14 nF and knowing the electrode area (0.197 cm^2) and polymer thickness (2 µm), the relative permittivity is calculated to be 13.1.

3.2. Sensor Characterization

The sensor electro-mechanical characterization is performed using TIRA shaker setup, shown in Fig.2(ii), and explained in [12]. The shaker tip applies the force with frequency 70 Hz and the magnitude of force is controlled using power amplifier. The sensor exploits the basic piezoelectric property of P(VDF-TrFE) of converting force into charge. A charge amplifier circuit shown in Fig. 2(iii), was designed to read this charge and convert into voltage. The force applied by the shaker was recorded with a force sensor and the output produced across the terminals of capacitive sensor was acquired by programmed Data Acquisition (DAQ) board, the characteristic curve can be seen in Fig.2 (iv). The sensors shows very good sensitivity of 80mV/N.

Conclusion

Piezoelectric capacitor using P(VDF-TrFE) polymer have been fabricated over bulk silicon, which is then thinned down to about 35 µm from original thickness of 636 µm using TMAH wet etching. This leads to bendable chip, which can conform to curved surfaces. The unpackaged chip shows a slight warpage of 1.6 µm which is expected due to stress generation after thinning. Future investigations will focus on methods to reduce this warpage effect. Thepiezoelectric capacitors on ultra-thin silicon substrate offer an attractive approach for sensors conforming to curved surface like humanoid hand part, prosthetic limbs etc.

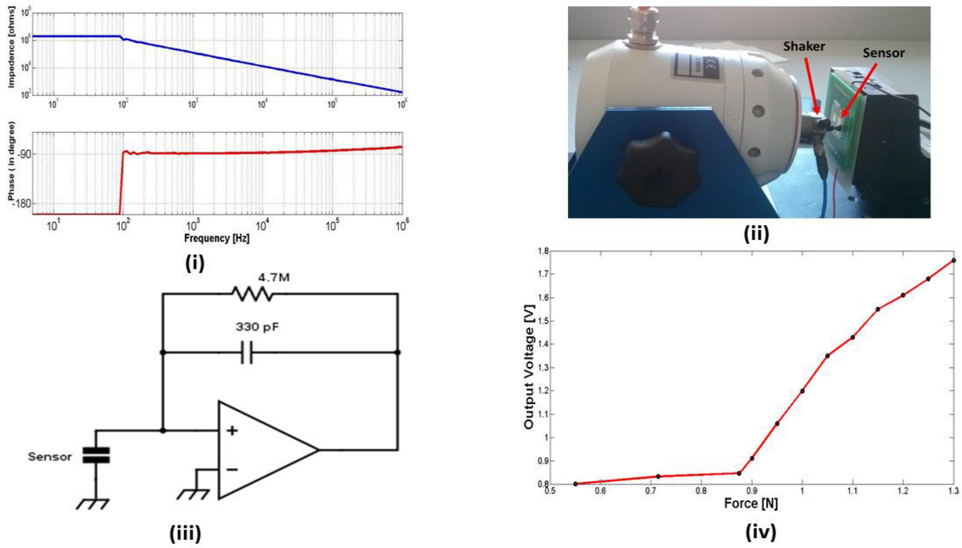

Fig.2: (i) Electrical impedance spectroscopy measurement, (ii) Sensor under test in the used measurement setup (iii) Schematic of charge amplifier circuit (iv) Sensor characteristic curve

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